CLAIMS

What is claimed is:

1. A system comprising:

a sample network that provides plural indications of signal state associated with different time instances of an input signal; and

a detector that provides an indication of a frequency for the input signal based on the plural indications of signal state.

2. The system of claim 1, the sample network further comprising a plurality of storage elements arranged to provide output samples corresponding to the plural indications of signal state.

3. The system of claim 2, further comprising delay elements associated with at least a substantial number of the storage elements, the delay elements providing respective delayed signals for activating the at least a substantial number of the storage elements to provide the plural indications of signal state to sample the input signal at different time intervals.

4. The system of claim 3, wherein the input signal is delayed by the delay elements to provide the respective delayed signals for activating the at least a substantial number of the storage elements.

5 The system of claim 2, further comprising an oscillator that provides a clock signal for activating at least a substantial number of the storage elements to provide the plural indications of signal state.

6. The system of claim 5, wherein the oscillator provides the clock signal at a frequency that is one of lower and higher than the frequency of the input signal.

7. The system of claim 5, further comprising delay elements associated with at least N of the storage elements, where N+1 is a positive integer denoting the number of the storage elements, the delay elements providing respective clock edges for activating the at least N of the storage elements, each of the clock edges corresponding to a different delayed version of the clock signal.

8. The system of claim 7, wherein the delay elements are connected in series so that the amount of delay for a given clock edge corresponds to an aggregate amount of delay according to the number of delay elements in the path from the oscillator to the storage element activated by the given clock edge.

9. The system of claim 8, wherein an output of a preceding storage element is coupled to an input of a next storage element.

10. The system of claim 8, wherein the input signal is provided to an input of each of the storage elements such that the storage elements provide the output samples based on activation by the given clock edge.

11. The system of claim 1, wherein the sample network further comprises a plurality of storage elements activated at time intervals to latch output samples concurrently to the detector corresponding to the plural indications of signal state.

12. The system of claim 1, further comprising:

a comparator that provides a comparator signal based on a comparison of the indication of frequency for the input signal and an indication of a desired frequency; and

a controller operative to implement adjustments to a clock signal based on the comparator signal.

13. The system of claim 12, further comprising an oscillator that generates the input signal as a clock signal having a frequency based on a controller output signal.

14. An integrated circuit chip comprising the system of claim 1.

15. A system comprising:

a plurality of storage elements, the plurality of storage elements being activated to latch different time instances of an input signal to provide corresponding output samples sufficient for determining frequency characteristics of the input signal.

16. The system of claim 15, further comprising a detector that provides an indication of frequency for the input signal based on the output samples.

17. The system of claim 15, further comprising a plurality of delay elements associated with at least a substantial number of the storage elements, the delay elements providing delayed signals for activating the at least a substantial number of the storage elements to provide the corresponding output samples.

18. The system of claim 17, wherein the input signal is delayed by the plurality of delay elements to provide respective delayed signals for activating the at least a substantial number of the storage elements.

19. The system of claim 17, wherein an output of a preceding storage element is coupled to an input of a next storage element.

20. The system of claim 15, further comprising an oscillator that provides a clock signal for activating the plurality of storage elements to provide the corresponding output samples.

21. The system of claim 20, further comprising delay elements associated with at least a substantial number of the storage elements, the delay elements providing respective delayed clock signals for activating the associated storage elements, each of the respective delayed clock signals corresponding to a different delayed version of the clock signal.

22. The system of claim 21, wherein the delay elements are connected in series so that the amount of delay for a given delayed clock signal corresponds to an aggregate amount of delay according to the number of delay elements in the path from the oscillator to the storage element activated by the given delayed clock signal.

23. The system of claim 22, wherein the input signal is provided to an input of each of the storage elements such that the storage elements provide the corresponding output samples based on activation by the respective delayed clock signals.

24. The system of claim 15, wherein the plurality of storage elements are activated at predetermined time intervals to latch the output samples to the detector concurrently to provide the corresponding output samples that represent different time instances of signal state for the input signal.

25. A frequency detection system comprising:

means for providing plural indications of signal state associated with different time instances of an input signal having an unknown frequency; and

means for determining an indication of frequency for the input signal based on the plural indications of signal state.

26. The system of claim 25, further comprising means for delaying sampling of the input signal by selected parts of the means for sampling.

27. The system of claim 25, wherein the means for delaying further comprises means for delaying a clock signal to provide activation signals that control sampling performed by the means for sampling.

28. The system of claim 25, wherein the means for sampling further comprising a plurality of means for storing signal state information based on an activation signal.

29. The system of claim 28, further comprising:

means for comparing the indication of frequency relative to an indication of a desired frequency; and

means for controlling the frequency of the input signal based on the comparison of the frequency of the input signal and the desired frequency.

30. A method comprising:

sampling a signal at predetermined spaced apart time intervals to provide a plurality of output samples indicative of signal state for different time instances of the signal; and

determining an indication of frequency for the signal based on the plurality of output samples.

31. The method of claim 30, the sampling further comprising activating a plurality of storage elements to provide the plurality of output samples concurrently.

32. The method of claim 31, the activation further comprising generating clock edges at spaced apart time intervals that are provided to activate the plurality of storage elements.

33. The method of claim 32, the generation of clock edges further comprising delaying a clock signal to provide the clock edges.

34. The method of claim 31, further comprising delaying propagation of the signal through the plurality of storage elements to establish the spaced apart time intervals at which the signal is sampled.

35. The method of claim 31 further comprising providing a clock signal to control the activation of the storage elements.

36. The method of claim 30, further comprising controlling an oscillator to provide the signal at a frequency based on a comparison of the indication of frequency for the signal relative to a desired frequency.

37. The method of claim 36, wherein the controlling further comprises providing at least one control signal to cause the oscillator to one of increase, decrease and not change the frequency of the signal.